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WHAT IS CLAIMED IS:

1. A method for refreshing a memory system having a predetermined number of memory blocks, the comprising:
 providing a system refresh signal for refreshing the memory system, the system refresh signal being used as a first refresh request signal for refreshing a first memory block;
 sequentially refreshing one or more subsequent memory blocks of the memory system,
 wherein all the memory blocks are refreshed within a retention cycle of the memory system.
2. The method of claim 1 wherein the providing further includes generating the system refresh signal by a refresh timer coupled to the first memory block.
3. The method of claim 1 wherein the sequentially refreshing further includes sequentially generating one or more refresh request signals for the subsequent memory blocks.
4. The method of claim 3 wherein the sequentially refreshing further includes providing a refresh request signal by a refresh control circuit in each subsequent memory block to its immediately subsequent memory block while it is undergoing a refresh operation.
5. The method of claim 4 wherein the sequentially refreshing further includes generating a refresh command based on the refresh request signal for refreshing each memory block.

6. The method of claim 4 wherein the refresh commands for the memory blocks do not overlap in timing.
7. The method of claim 3 wherein the refresh requests do not overlap in timing.
8. A memory system comprising:
a first memory block coupled to a refresh timer; and
one or more subsequent memory blocks without refresh timers contained therein,
wherein the refresh timer generates a system refresh signal for refreshing the memory system, and
wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks.
9. The memory system of claim 8 wherein the refresh controller of the first memory block receives the system refresh request generated by the refresh timer.
10. The memory system of claim 8 wherein the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block.
11. The memory system of claim 10 wherein the refresh controller of each memory block generates a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed.
- ~~12~~¹². The memory system of claim 10 wherein the refresh requests generated do not overlap in timing.

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~~14.~~ The memory system of claim 10 wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to.

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~~15.~~ The memory system of claim 14 wherein the refresh commands generated do not overlap in timing.

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~~16.~~ The memory system of claim 8 wherein the refresh controller provides a refresh address.

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~~17.~~ A dynamic random access memory system comprising:
a first memory block coupled to a refresh timer; and
one or more subsequent memory blocks without refresh timers contained therein,

wherein the refresh timer generates a system refresh signal for refreshing the memory system, and

wherein all memory blocks have a refresh controller contained therein which enable sequential refresh of the subsequent memory blocks.

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~~18.~~ The memory system of claim 17 wherein the refresh controller of the first memory block receives the system refresh request generated by the refresh timer.

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~~19.~~ The memory system of claim 17 wherein the refresh controller of each memory block generates a refresh command for refreshing the memory block it belongs to and a refresh request for an immediately subsequent memory block when the memory block it belongs to is being refreshed.

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~~20.~~ The memory system of claim 19 wherein the refresh requests generated do not overlap in timing.

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~~21.~~ The memory system of claim 19 wherein the refresh commands generated do not overlap in timing.

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~~22.~~ The memory system of claim 17 wherein the refresh controller provides a refresh address.